**Lab Exercise Two**

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**Step 1**

Write the SystemVerilog module for the Gray Code Converter that we developed in a previous class (10 pts).

Here are the simplified equations:

G = x

H = x’y + xy’

I = y’z + yz’

**module** LabExerciseTwo(a, b, c, G, H, I );

**input** a, b, c;

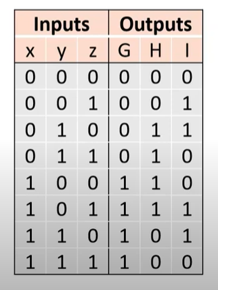
**output** G, H, I;

**assign** G = a; **//G = x**

**assign** H = ~a & b | a & ~b; **//H = x’y + xy’**

**assign** I = ~b & c | b & ~c; **//I = y’z + yz’**

**endmodule**

**Step 2**

Based on the following truth table create a self-checking testbench to test the SystemVerilog code created Step 1. The testbench must test all rows in the truth table (30 pts).

Hint: Use the 2x4 Decoder testbench covered in class on 10/12 as a guide.

**module** LabExerciseTwo\_tb;

**reg** a, b, c;

**wire** G, H, I;

LabExerciseTwo l2(.a(a),.b(b),.c(c),.G(G),.H(H),.I(I));

**initial begin**

$dumpfile("dump.vcd");

$dumpvars(1);

a=0; b=0; c=0;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 0 & H== 0 & I== 0) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

a=0; b=0; c=1;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 0 & H== 0 & I== 1) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

a=0; b=1; c=0;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 0 & H== 1 & I== 1) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

a=0; b=1; c=1;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 0 & H== 1 & I== 0) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

a=1; b=0; c=0;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 1 & H== 1 & I== 0) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

a=1; b=0; c=1;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 1 & H== 1 & I== 1) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

a=1; b=1; c=0;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 1 & H== 0 & I== 1) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

a=1; b=1; c=1;

**#1**

**//$display("a:%b,b:%b,c:%b -> G:%b,H:%b,I:%b ",a,b,c,G,H,I);**

if (G == 1 & H== 0 & I== 0) $display("%b%b%b passed", a,b,c); else $error("%b%b%b failed", a,b,c);

**end**

**endmodule**

**Compiled example:**

A screenshot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated**With results un-comented to check truth table:**